REMARKS/ARGUMENTS

Claims 1-37 are pending.

Claims 1-27 were rejected under 35 U.S.C. § 101 for allegedly being drawn to non-statutory subject matter.

Claims 1-37 were rejected under 35 U.S.C. § 103(a) for allegedly being unpatentable over U.S. Patent No. 6,571,268 to Giacalone et al. in view of U.S. Patent Application Publication No. 2002/0039386 to Han et al.

Section 101 Rejection

Claim 1 has been amended to recite providing left and right memory banks and a summing circuit. Claim 1 further recites configuring logic circuits to store intermediate result data produced by the summing circuit into the left memory bank and the right memory bank in a manner to simulate a layered tree structure. Since claim 1 recites a step of configuring logic circuits, the steps in claim 1 are no longer merely drawn to mental processes. The Section 101 rejection of claims 1-13 is believed to be overcome.

Claim 14 has been amended to address the Section 101 rejection. As amended, claim 14 is directed to a method of operating an accumulator to accumulate initial input values. Claim 14 recites streaming initial input values to "an input of the accumulator." As originally filed, claim 14 recited "directing said adder output value to one of a memory bank and a result queue" which is an action that is carried out by an apparatus, namely a memory bank and a result queue, which is believed to be statutory subject matter. Nonetheless, claim 14 has been further amended to recite "directing said adder output value to one of a memory bank of said accumulator or a result queue of said accumulator" to more clearly recite the steps as being directed to actions on physical structures; i.e., the claimed method sets forth a machine, namely "an accumulator." The recited steps are no longer merely drawn to mental processes. The Section 101 rejection of claims 14-27 is believed to be overcome.

Section 103 Rejection

The pending independent claims are claims 1, 14, and 28.

Independent claim 1 recites a method of constructing an accumulator. Among other things, claim 1 recites providing a left memory bank and a right memory bank, and configuring logic circuits to store intermediate result data into the left memory bank and into the right memory bank in a manner to simulate a layered tree structure. Fig. 5 of the pending specification shows an example of the layered tree structure arrangement.

Giacalone et al. describe a multiplier/accumulator circuit (MAC). Figs. 1, 2, and 20 (cited in the Office action) show high level blocks of a MAC unit. For example, in Fig. 2 the Booth stages relate to generating partial products. The Wallace tree stages relate to summing the partial products. A final adder stage (140) is also shown. Giacalone et al. show in Figs. 5A and 5B the alignment of partial products in their Wallace tree stages. The figures do not show storage of intermediate result data in a left memory bank and a right memory bank in a manner to simulate a layered tree structure. Giacalone et al. therefore do not show or suggest that their Wallace tree stages or their final adder (140) configuring logic circuits to store intermediate result data into the left memory bank and into the right memory bank in a manner to simulate a layered tree structure.

Independent claim 14 recites, among other things, streaming initial input values to an input. Claim 14 further recites selecting a left side source from among a zero value, the initial input values, or a set of intermediate result values. Claim 14 further recites selecting a right side source from among a zero value, the initial input values, or a set of intermediate result values. Claim 14 further recites adding the left side source and the right side source. Claim 14 further recites directing the result to one of a memory bank of said accumulator or a result queue of said accumulator. See also **independent claim 28**.

Giacalone et al. describe a multiplier/accumulator circuit (MAC). Figs. 1, 2, and 20 (cited in the Office action) show high level blocks of a MAC unit. For example, in Fig. 2 the Booth stages relate to generating partial products. The Wallace tree stages relate to summing the partial products. A final adder stage (140) is also shown. Figs. 1 and 2, however, do not show or

suggest selecting a left side source (or selecting a right side source) from among a zero value, the initial input values , or a set of intermediate result values. Giacalone et al. do not show or suggest that their Wallace tree stages or their final adder (140) are configured to add the left side source and the right side source, and direct the result to one of a memory bank of the accumulator or a result queue of the accumulator.

Fig. 21 (cited in the Office action) shows a MAC unit (100) interconnected with various busses for data source and destination. *Col. 25, lines 30 and following.* Fig. 21 also shows a second MAC unit. As understood, Giacalone et al. do not show or suggest in Fig. 21 the recited selecting a left side source from among a zero value, the initial input values, or a set of intermediate result values. Fig. 21 does not show or suggest adding the left side source and the right side source, and directing the result to one of a memory bank of said accumulator or a result queue of said accumulator as recited in claim 14 and similarly in claim 28.

Fig. 22 (cited in the Office action) shows an arrangement of accumulator registers for moving data into the MAC units of Fig 21. *Col. 25, lines 57-67.* Fig. 22 does not show or suggest the recited selecting a left side source from among a zero value, the initial input values, or a set of intermediate result values, nor the recited adding the left side source and the right side source, and directing the result to one of a memory bank of said accumulator or a result queue of said accumulator.

Fig. 17C (cited in the Office action) shows, along with Figs. 17A and 17B, saturation circuits used to generate saturation values for overflow conditions. *Col. 22, lines 41-48.* It is not clear how Fig. 17C shows or even suggests selecting a left side source from among a zero value, the initial input values, or a set of intermediate result values.

As to the Han et al. reference, the reference does not show or suggest the foregoing discussed recited aspects of claim 14 or claim 28. Han et al. show in Fig. 10 the structure of a first level accumulator (see Fig. 6). *Paragraph [0059].* Fig. 11 shows the structure of a second level accumulator. *Paragraph [0060].* Neither Fig. 10 nor Fig. 11 shows or suggests selecting a left side source from among a zero value, the initial input values, or a set of intermediate result values. The figure does not show adding the left side source and the right

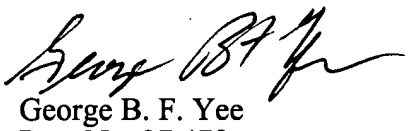
side source, and directing the result to one of a memory bank of said accumulator or a result queue of said accumulator.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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